TEST SYSTEM FOR MULTI-PROCESSOR SYSTEM

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Abstract of **JP59055549**

PURPOSE:To facilitate easy execution of a test for a multi-processor system, by applying an interruption to one of plural processors from a test device to obtain a test mode, and storing the result of test into a shared circuit via a shared bus. CONSTITUTION:Plural processors 1-3 and a common memory 130 are connected to common buses 111-113, a data bus 6 and an address bus 7 via a bus control circuit 4. While a test device 5 applies an interruption to a processor to be tested via a tester interruption informing line 8. A test program 131 which controls the device 5 is stored in the memory 130. Each of processors 1-3 requests a common bus access to the circuit 4 when detecting own address from an interruption signal. Thus the processor obtains its own test mode and sends the data to the device 5 via a test response line 120. In such a way, it is possible to have an effective test of many processors with just a single tester.